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CURRENT BALANCING IN MULTIPHASE CONVERTER BASED ON INTERLEAVING TECHNIQUE USING FUZZY LOGIC

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ABSTRACT

In the field of power electronics, multiphase converter is used to achieve fast dynamic response, smaller filters and better packaging. Typically, multiphase buck converter have several paralleled power stages with current loops to increase dynamic response using current mode control and to avoid current unbalance among phases. The proposed multiphase converter based on interleaving technique results in cancellation of the current ripple generated at the output of each converter cell. The interleaving technique provides an intrinsic self-balance mechanism which is used to avoid the current unbalance. In addition fuzzy logic has been implemented on multiphase buck converter to achieve dynamic voltage regulation and better current balance.

KEYWORDS: Multiphase buck converter, dynamic response, current unbalance, fuzzy logic.

INTRODUCTION

A switching converter is an electronic power system which transforms an input voltage level into another for a given load by a switching action of semiconductor devices. A high power efficient dc-dc converter is strongly desired and has found widespread applications.

Typically, the power of this converter ranges from 500 to 1000 W. Due to the relative high current of this application; some approaches use the interleaving technique [1]. The main advantages of using this technique in this application are the filter's reduction and efficiency. State of the art engineering for this application proposes the use of three to five paralleled buck stages (phases) to build the converter. A comparison between these multiphase converters with a single buck converter is carried out in [2], where the advantage of this technique for this application can be seen. Reference [3] proposes a CAD tool to calculate the number of phases to optimize cost, size, and weight. A similar analysis, but more oriented to calculate power losses, can be found in [4]. A magnetic component to couple all the phases is introduced in [5], obtaining a size reduction compared with inductors form the same power losses. A quite different solution is presented in [6], where the authors propose a multilevel converter to decrease the voltage stress in the transistors and to eliminate the inductor.

Using interleaving, the power stage of a converter is divided into several and smaller power stages. Therefore, the size of each component is reduced. With a very high number of interleaved phases, the current stress is greatly reduced and using a different technology becomes a possibility.

However, there are some challenges to face a many-phase converter.

General purpose integrated circuits (ICs) cannot be used because there are many phases. Specific digital control is required.Introducing a current loop per phase will not be cost-effective. Passive current equalization should be considered.

The multiphase synchronous buck converter, as shown in Fig. 1, is widely adopted in the VR design [7], [8]. Many papers have discussed the multiphase VR's transient response and how to improve it [9]–[13]. It has been shown that the feedback control loop's bandwidth plays a very important role in the transient response. With a higher bandwidth, fewer output capacitors are needed for the required transient performance [12], [13].

In CCM (Continuous Conduction Mode), the current unbalance depends mainly on duty cycle differences and parasitic resistance [14]. In most cases these parameters are under certain limits allowing the operation of the converter without the aforementioned current loops.

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Since the duty cycle is the main responsible of the current unbalance, it is especially important the use of digital control that reduces the inequalities of the driving signals of the power MOSFETs. The use of a high number of phases together with digital control without current loops have been used successfully in static conditions [15].

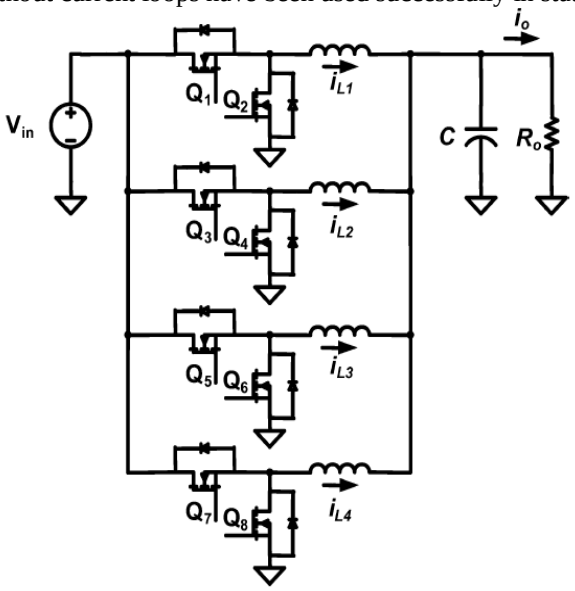

Fig. 1. Multiphase synchronous buck converter.

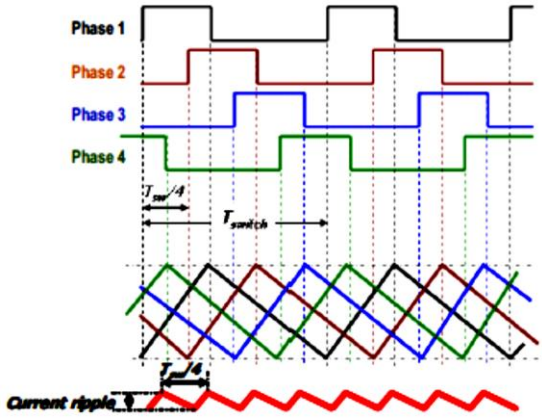

Fig. 2. Main waveforms in steady-state conditions

The objective of this paper is to propose a design for the power stage in CCM that improves the current balance without using current loops. If this were possible, designs with a high number of phases would become a realistic option in some applications.

CURRENT BALANCING

One of the concerns of the interleaved converters is current balancing. Commercial integrated circuits solve this problem by including an additional current loop [16], [17]. As a consequence, the cost of the IC is quite high. Also, the additional circuitry grows, increasing size and decreasing reliability. Therefore, although the aforementioned IC controllers have been designed with the capability of paralleling some of them, in practice, a high number of phases are not feasible.

The purpose of this paper is to use a high number of phases but without any current loop. The dc current depends strongly on the conduction mode of the converter.

A. Continuous Conduction Mode (CCM)

Figure 3 shows the equivalent dc circuit of a multiphase buck converter when it operates in CCM. Each phase is characterized by a dc parasitic resistance (R_i); the voltage applied to this resistance is the input voltage (V_{IN}) multiplied by the actual duty cycle of this phase (d_i).

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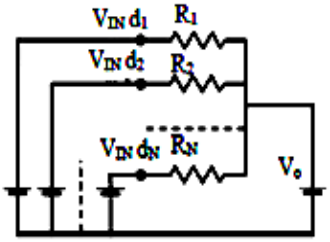

Fig. 3. Equivalent dc circuit of the multiphase buck converter working in CCM.

In case of passive load (R_o), the output voltage of the converter (V_O) can be calculated from the aforementioned parameters
(V_{IN}, d_i, and R_i) with the following expression:

$$V_O = \frac{\sum_1^n \frac{V_{IN} d_i}{R_i}}{\frac{1}{R_O} + \sum_1^n \frac{1}{R_i}} \qquad (1)$$

Note that if the load is a battery, the output voltage is just the battery voltage and (1) is not used. Once V_O is known, the current through each phase is easily calculated

$$I_i = \frac{V_{IN} d_i - V_O}{R_i} \qquad (2)$$

The worst-case for a single phase takes place when this phase has the maximum duty cycle and the minimum resistance while the rest have minimum duty cycle and maximum resistance. In such a case, the phase current is maximum while the other phases will handle a current below the average value Io /N. In order to determine which of both factors (differences in duty cycle or in resistance) is the most important, we can analyze each one independently. This analysis can be found in detail in [17], but the main results are the following ones. The differences caused by resistance unbalance when only one resistance is different from the others can be calculated as shown in

$$\left(\frac{\Delta I_i}{I_i}\right)_R = -\frac{N-1}{N}\frac{\Delta R}{R} \qquad (3)$$

being R the common resistance for the rest of the phases and ΔR the difference in the unbalanced resistance. On the other hand, the differences caused by duty cycle unbalance when only one duty cycle is different from the others can be calculated as shown in

$$\left(\frac{\Delta I_i}{I_i}\right)_d = -\frac{N-1}{N}\frac{1}{1-\eta}\frac{\Delta d}{d} \qquad (4)$$

being d the common duty cycle for the rest of the phases, Δd the difference in the unbalanced duty cycle, and η the power efficiency due to losses on the resistance exclusively.

In order to compare both factors, a numerical example is analyzed. For a 16-phases converter with 98% efficiency due to resistance (2% losses in the resistance), a 10% difference in one of the resistances causes less than a 10% difference in the current of that phase. However, for the same converter a minimum 1% difference in one of the duty cycles causes a 47% unbalance in the current of the unbalanced phase. As it can be seen, duty cycle is responsible for the main current unbalance unless the resistance causes very high losses (over 10%), which is avoided by design. Regarding the inductor value, its differences cause only unbalanced current ripples (peak to peak), but the dc current per phase is unaffected in CCM. However, it affects dc current in discontinuous conduction mode (DCM), as explained in the next point.

Therefore, it can be stated that duty cycle is the main cause of current unbalance in CCM. However, the use of digital control drastically reduces unbalances caused by duty cycle, because the driving signal is generated with great accuracy

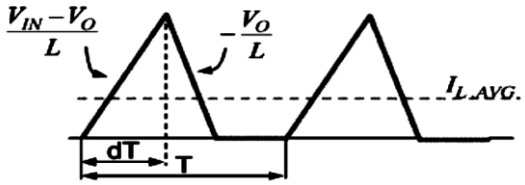

Fig. 4. Inductor current in DCM

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(Differences below 1 ns). Differences in duty cycle of the phases will be produced by drivers and MOSFETs variations (so they should be chosen taking this into account). Thus, in many cases, it is possible to eliminate current sensing circuits, current loops, and all the associated circuitry. In conclusion, the control stage is composed of a single voltage loop and driving signals generator, making it feasible to build a multiphase converter with many phases (more than the classical three or four) at a reasonable cost.

In the experimental results section, the converter has been designed without current loops trusting in the digital control for current equalization. It will be seen that it is not necessary to include this current loop.

B. Discontinuous Conduction Mode (DCM)

DCM is a very interesting option for multiphase converters because the equalization of the currents is much better. Inductor current of a single phase in a switching cycle is shown in Fig. 6.

The average value of the inductor current (output current of a phase) can be calculated from Fig. 4 and is defined in

$$I_{i,AVG} = \frac{V_{IN} d_i^2}{2Lf}\left(\frac{V_{IN} - V_O}{V_O}\right) \qquad (5)$$

and even a 5% difference in duty cycle causes just a 10% current unbalance. Regarding the inductor value, a 10% difference causes a 9% current unbalance, and even a 20% difference in inductance causes just a 17% current unbalance.

SELF-BALANCE OF THE PHASE CURRENTS

Each buck converter has two switches (see figure 5): the one that connects the input to the inductor (high side MOSFET or HSM); and the one that connects the inductor to ground (low side MOSFET or LSM). ZVS is achieved naturally in the turn-on of LSM with a proper timing of the gate signals of these transistors. In typical designs, the turn-on of the HSM is dissipative since the inductor current is always positive and there is no way to charge/discharge the parasitic capacitances.

In case of designing the converter to have negative current in that transition, ZVS is achieved, with a similar mechanism. It will be seen that this also helps to improve the current balance without current loops.

To explain the auto-balance of the currents, several images of the turn-off of the LSM taken with the oscilloscope are shown in figure 6. In four different conditions, V_{GS}_LSM, V_{DS}_LSM and i_L are shown.

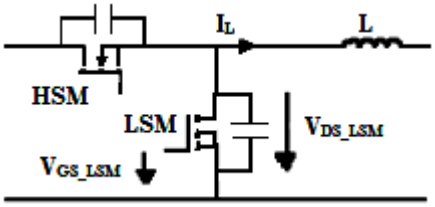

Fig. 5. Power transistors and inductor of the synchronous buck converter. Parasitic capacitances have been drawn

When the turn-on of HSM takes place with ZVS, the speed of the charge/discharge of the parasitic capacitances is determined by the instantaneous inductor current and not by the gate-source signal of HSM. Therefore, a more (instantaneous) negative current produces a quicker transition increasing the voltage second balance on the inductor and then increasing the average inductor current. This mechanism tries to compensate current unbalances since the phase with the smallest dc current polarizes more its inductor and, as a consequence, the dc current is increased.

Figure 6d shows the V_{DS}, LSM voltage with no ZVS because instantaneous inductor current is positive. In the other three cases fig 6a, 6b and 6c, there is ZVS. It can be clearly seen that the higher the negative current, the shorter the switching interval (around 40 ns in fig.6a)

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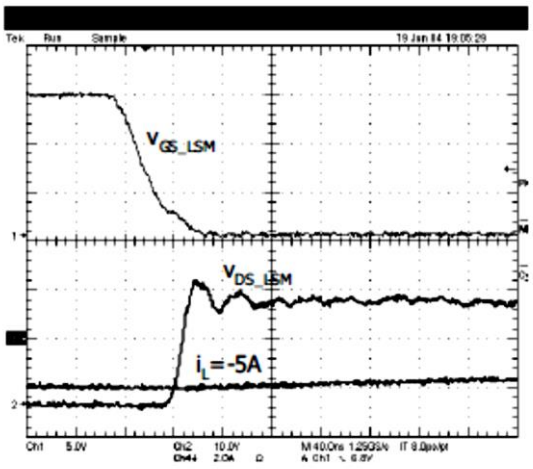
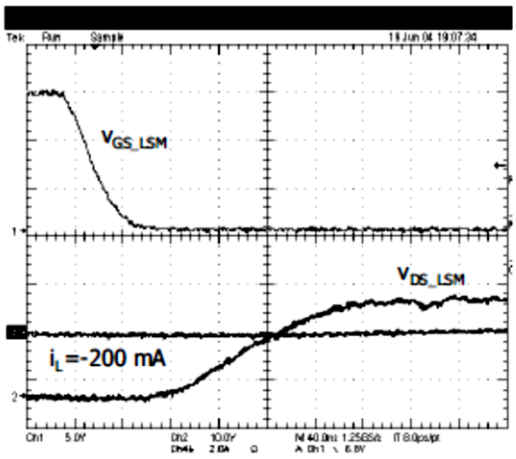
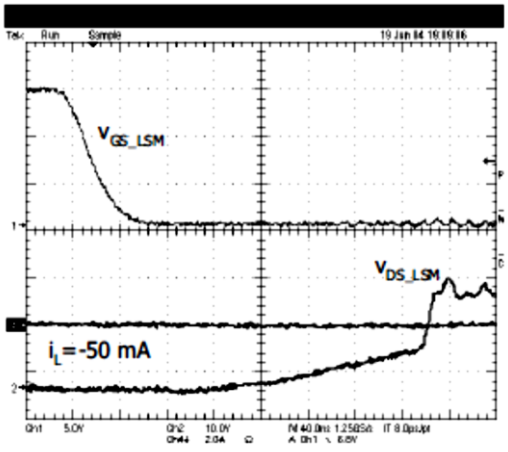


(a)



(b)



(c)

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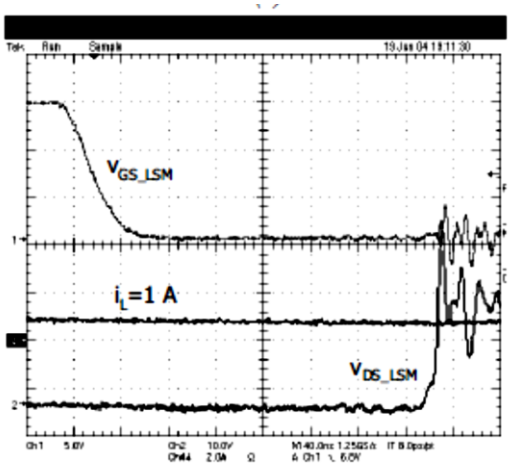

(d)

Fig. 6. Gate to source voltage of the LSM (5V/div), drain to source voltage of the LSM (10V/div) and inductor current (2A/div) for four different instantaneous inductor currents: (a) -5A (b) -0.2A (c) -0.05A (d) +1A

On the other hand, the smaller (but negative) the instantaneous current, the higher the switching interval. This is a well-known issue but the important thing is that this fact helps to compensate different dc currents in a multiphase converter. Thus, the phase with the most negative current changes its inductor voltage faster and, therefore, it tries to increase its average current value.

EXPERIMENTAL VERIFICATION

A 4-phases synchronous buck converter without current loops has been built and tested. The main specifications are: V_{IN}=28V; V_O=12V; P_O=60W; and f_S=250 kHz. The inductor has been designed to obtain a current ripple higher (but close) to 200% of the average phase current (current ripple equal to 2.5A being 1.25A the average phase current). In this condition, the instantaneous phase current is negative once the LSM is opened.

A. System Design without PI Controller

Without PI controller the output phase currents of multiphase synchronous buck converter is unbalanced. A four phase buck converter simulated output waveforms are shown in fig. 7.

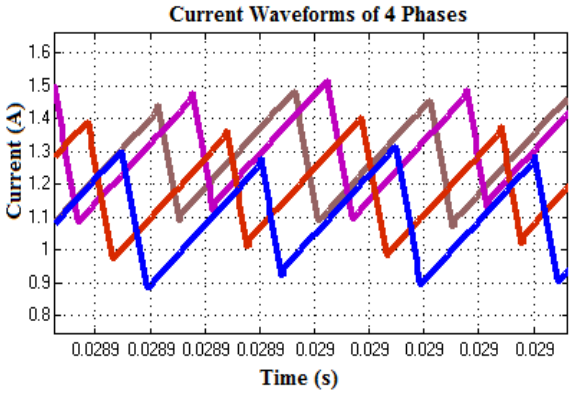

Fig. 7. Individual phase current of the converter system without PI controller

B. System Design with PI Controller

Feedback is used in control systems to change the dynamic behaviour of the system. The control strategy of the proposed converter is based on voltage-mode-controlled Pulse Width Modulation (PWM) with a Proportional and Integral (PI) controller which takes its control signal from the output voltage of the switching converter instead of current-mode (or current-injected) PWM, which utilizes both the output voltage information and the current information from the inductor to determine the desired duty cycle.

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Simulink model for multiphase buck converter with PI controller is shown in Fig. 8 and output phase current waveforms are shown in Fig. 9. By using PI controller we get almost balanced phase currents.

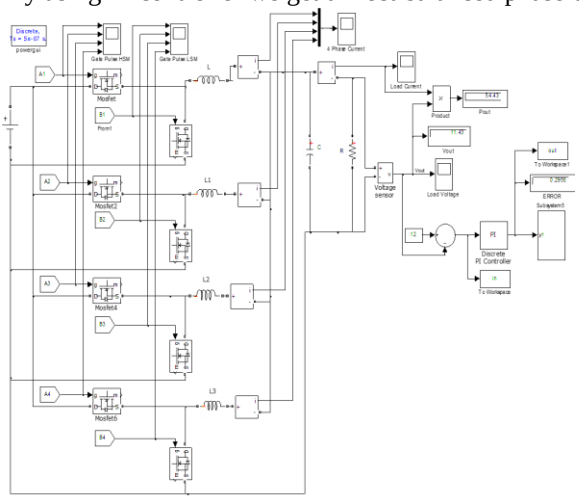

Fig. 8. Simulink model for multiphase buck converter with PI controller

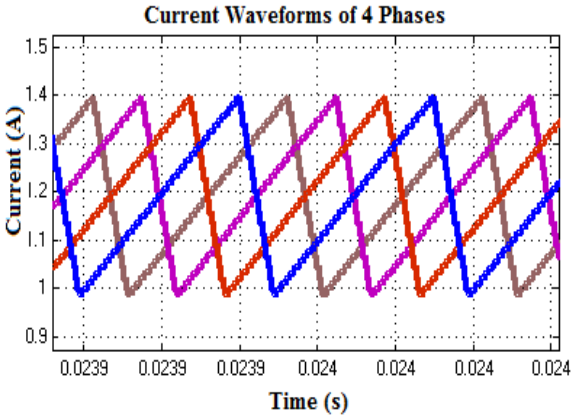

Fig. 9. Individual phase current of the converter system with PI controller

C. System Design with Fuzzy Logic Controller

Fuzzy set theory has been widely used in the control area with some application to dc-to-dc converter system. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab /Simulink simulation model is built to study the dynamic behavior of dc-to-dc converter and performance of proposed controllers. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not possible with linear control technique. Thus, fuzzy logic controller has potential ability to improve the robustness of dc-to-dc converters. The fuzzy approach offers the possibility to model a non–linear system on the basis of the knowledge of many non-well defined relations among the variables of the system, and to design a controller that adapts itself to several working conditions.

In an FLC the dynamic behavior of a fuzzy system is characterized by a set of linguistic description rules based on expert knowledge. The expert knowledge is usually of the form "IF (a set of conditions are satisfied) THEN (a set of consequences can be inferred)".

Since the antecedents and the consequents of these IF-THEN rules are associated with fuzzy concepts, they are often called fuzzy conditional statements. In our terminology, a fuzzy control rule is a fuzzy conditional statement in which the antecedent is a condition in its application domain and the consequent is a control action for the system under control. Basically the fuzzy control rules provide a convenient way for expressing control policy and domain knowledge. Furthermore, several linguistic variables might be involved in the antecedents and the conclusions of these rules. When this is the case the system will be referred to as a multi-input-multi-output (MIMO) fuzzy system.

The Fig. 10 shows membership functions for error, change in error and output variable:

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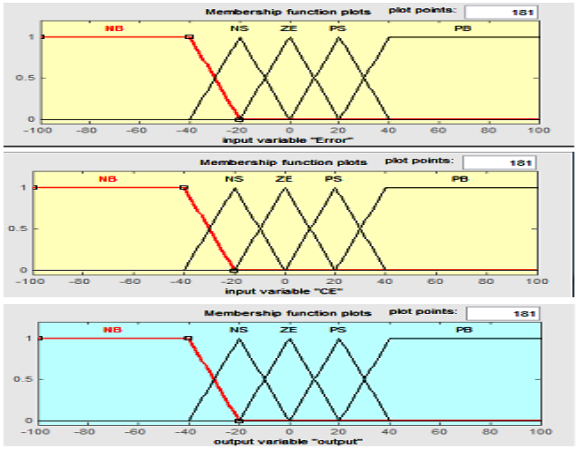

Fig. 10. Input and output membership functions

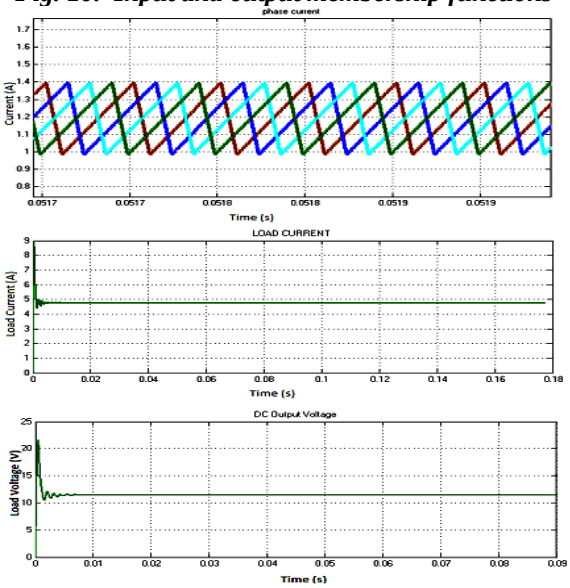

Fig. 11. Individual phase currents then total output current and bottom trace is the output voltage of the converter system with fuzzy logic control

CONCLUSIONS AND FUTURE SCOPE OF THE WORK

The Multiphase buck converter has one current loop per phase to achieve current balance and dynamic response. Two important issues are achieved: both current balance and zero voltage switching. Intrinsic self balance mechanism tries to compensate current unbalances. The main advantage of this approach is that phase current is cancelled obtaining advantage in filter reduction and dynamic response. The fact of having M current loops limits the existence of multiphase converter with a high number of phases.

This paper presents the current balancing technique using multiphase buck converter. This can be implemented in hardware to verify the simulation results. Also Current Balancing using multiphase boost converter will be simulated in future.

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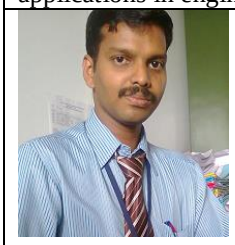

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